global word line decoder 620. Each global word line decoder 620a-d is activated when predecoder 622 transmits address information relevant to a particular global word line decoder 620a-d via predecoder lines 623. In response, global word line decoder 620a-d activates global word line 630 which, in turn, activates a particular local word line decoder 615a-c. Local word line decoder 615a-c then enables associated memory module 605, so that the particular memory cell 610 of interest can be evaluated. Each of memory modules 605 can be considered to be an independent memory component to the extent that the hierarchical functionality of each of modules 605 relies upon local sensing via local sense amplifiers 608a-b, local decoding via local word line decoders 615a-c, or both. Global sense amplifiers (GSA), such as GSA 640, also are shown. As with other preferred embodiments of the invention herein, it is desirable to have each module 605 be self-timed. Self-timing can be especially useful when used in conjunction with local word line decoding because a local timing signal from a respective one of memory module 605 can be used to terminate global word line activation, local bitline sensing, or both.

Kindly delete the paragraph beginning "FIG. 8" at page 32, line 17 and ending "buffer delay" at page 32, line 25, and replace it with the following paragraph:

FIG. 8 is a circuit diagram illustrative of an asynchronously-resettable decoder 800 according to this aspect of the present invention. FIG. 8 illustrates PMOS transistors M5, M6, M7, M8, M10, M11, M12, M13 and M14, and NMOS transistors M0, M1, M2, M3, M4 and M16. Inverters I12 and I13 also are connected as shown. It may be desirable to implement the AND function, for example, by source-coupled logic. The capacitance on the input x2_n 802 can be generally large, therefore the AND function is

performed with about one inverter delay plus three buffer stages. The buffers are skewed, which decreases the load capacitance by about one-half and decreases the buffer delay.

Kindly delete the paragraph beginning "In FIG. 12," at page 36, line 13 and ending "in the art" at page 36, line 34, and replace it with the following paragraph:

In FIG. 12, memory structure 1200, composed of hierarchical functional memory modules 1201 is preferred to have at least one or more redundant memory rows 1202, 1204; one, or more redundant memory columns 1206, 1208; or both, within each module 1201. It is preferred that the redundant memory rows 1202, 1204, and/or columns 1206, 1208 be paired, because it has been observed that bit cell failures tend to occur in pairs. Module-level redundancy, as shown in FIG. 12, where redundancy is implemented using a preselected number of redundant memory rows 1202, 1204, or redundant memory columns 1206, 1208, within memory module 1201, can be a very area-efficient approach provided the typical number of bit cell failures per module remains small. By implementing only a single row 1202 or a single column 1206 or both in memory module 1201, only one additional multiplexer is needed for the respective row or column. As explained in connection with FIG. 6, each global word line decoder (GWD) is activated when a predecoder transmits address information relevant to a particular GWD via precoder lines. Although it may be simpler to provide redundant memory cell circuits that can be activated during product testing during the manufacturing stage, it may also be desirable to activate selected redundant memory cells when the memory product is in service, e.g., during maintenance or on-the-fly

B3 Contd during product operation. Such activation can be effected by numerous techniques and support circuitry which are well-known in the art.

Kindly delete the paragraph beginning "FIG. 17" at page 39, line 32 and ending "and 1702" at page 40, line 15, and replace it with the following paragraph:

B4 FIG. 17 illustrates a preferred embodiment of selector 1600 in FIG. 16, in the form of decoder 1700 with row redundancy as realized in a hierarchical memory environment. Decoder 1700 may be particularly suitable for implementing module-level redundancy, such as that described relative to module 1200 in FIG. 12. Global decoder 1700, can operate similarly to the manner of asynchronously-resettable decoder 800 of FIG. 8. As shown in FIG. 17, decoder 1700 includes inputs shift, shift_n_Prev, xL_Prev, x1, x2_n, x2_n_Prev, shutInH (1703), shift_n, and outputs xL_Next, shutoutH, and WL. In general, decoder 1700 can be coupled with a first, designated memory row, and a second, alternative memory row. Although the second row may be a physical row adjacent the first memory row, and another of the originally designated rows of the memory module, the second row also may be a redundant row which is implemented in the module. Although row decoder 1700 decodes the first memory row under normal operations, it also is disposed to select and decode the second memory row in response to an alternative-row-select signal. Where the second row is a redundant row, it may be more suitable to deem the selection signal to be a "redundant-row-select" signal. The aforementioned row select signals are illustrated as inputs 1701 and 1702.

In The Claims:

Kindly amend claims 1, 6, 12 and 13 as follows:

1. (Twice Amended) An address decoder for a memory cell, comprising:

a. a synchronous portion, disposed to receive and respond to a clocked signal;

B5

b. an asynchronous portion, coupled with a line for the memory cell; and

c. a feedback-resetting portion comprising an input receiving an input signal from the asynchronous portion and an output transmitting an output signal to the synchronous portion in response to the input signal, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal.

6. (Twice Amended) A decoder in a memory module having a plurality of memory cell groups, comprising:

B6

a. a signal input;

b. a first memory output coupled with a first memory cell group;

c. a second memory output coupled with a second memory cell group; and

d. a selector coupled between the signal input, the first memory output, and the second memory output, wherein in the event of a fault detected on the first memory output when the decoder is in service, the decoder decodes an address to enable the second memory cell group responsive to a group-select signal.

12. (Twice Amended) A decoder in a memory module having a plurality of memory cell groups, comprising:

a. a synchronous portion, disposed to receive and respond to a clocked signal;

b. an asynchronous portion, coupled with a selected memory cell group;

B7

c. a feedback-resetting portion comprising an input receiving an input signal from the asynchronous portion and an output transmitting an output signal to the synchronous portion in response to the input signal, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal;

d. a signal input;

e. a first memory output coupled with a first memory cell group;

f. a second memory output coupled with a second memory cell group; and

g. a selector coupled between the signal input, the first memory output, and the second memory output, wherein in the event of a fault detected on the first memory output when the decoder is in service, the decoder decodes an address to enable the second memory cell group responsive to a group-select signal.